AMENDMENTS TO THE CLAIMS

1. (Currently amended) A current regulation circuit, comprising:

a current mirror arranged with a sense transistor and a power transistor;

a current sink that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense transistor ~~resistor~~ if a current flowing through the power transistor is less than a limit; and

a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to a drain voltage of the power transistor.

2. (Currently amended) The circuit of Claim 1, further comprising a component that outputs a signal if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to the drain voltage of the power transistor.

3. (Original) The circuit of Claim 2, wherein the component is at least one of a comparator and a differential amplifier.

4. (Original) The circuit of Claim 2, wherein the control component employs the signal to substantially turn off the current flowing through the power transistor.

5. (Original) The circuit of Claim 2, wherein the control component employs the signal to modulate the amount of current flowing through the power transistor to be less than the limit.

6. (Original) The circuit of Claim 1, wherein the control component senses a feedback signal provided by a load coupled to a drain of the power amplifier, wherein the feedback signal is employed in the control of the operation of the control component.

7. (Currently amended) The circuit of Claim 1, wherein the current mirror of the power transistor and the sense transistor ~~resistor~~ employs a ratio of m:1.

8. (Currently amended) The circuit of Claim 1, wherein the sense transistor ~~resistor~~ and the power transistor are at least field effect transistors (FET).

9. (Currently amended) A current regulation circuit, comprising:

a current mirror arranged with a sense transistor and a power transistor;

a current sink that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense transistor if a current flowing through the power transistor is less than a limit;

a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense transistor is substantially equivalent to a drain voltage of the power transistor; and

~~The circuit of Claim 1, further comprises~~ a clock signal that enables the regulation of a switching current flowing through the power transistor.

10. (Currently amended) The circuit of Claim 9, further comprising a first switch and a second switch for controlling a switching current that flows through the power transistor, wherein the first switch enables an output of the control component to be coupled to at least the power transistor and the sense transistor and wherein the second switch enables an output from a comparison component to be coupled to the control component, and wherein the comparison component's output indicates if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to a drain voltage of the power transistor.

11. (Currently amended) The circuit of Claim 10, wherein the first switch is arranged in an open state and the second switch is arranged in an open state if the switching current flowing through the power transistor and another switching current flowing through the sense transistor ~~resistor~~ are both substantially equivalent to zero.

12. (Currently amended) A current regulator, comprising:

a current mirror arranged with a sense transistor and a power transistor;

a current sink that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense transistor ~~resistor~~ if a current flowing through the power transistor is less than a limit;

a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to a drain voltage of the power transistor; and

a comparison component that presents a signal if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to the drain voltage of the power transistor.

13. (Original) The current regulator of Claim 12, further comprises a clock signal that enables the regulation of a switching current flowing through the power transistor.

14. (Currently amended) A current regulator, comprising:

a current mirror arranged with a sense transistor and a power transistor;

a current sink that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense transistor if a current flowing through the power transistor is less than a limit;

a control component that is arranged to limit the current flowing through the power transistor if the drain voltage of the sense transistor is substantially equivalent to a drain voltage of the power transistor;

a comparison component that presents a signal if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to the drain voltage of the power transistor; and~~The current regulator of Claim 12, further comprising~~

a first switch and a second switch for operating with a switching current flowing through the power transistor, wherein the first switch enables an output of the control component to be coupled to at least the power transistor and the sense transistor and wherein the second switch enables signal

presented by the comparison component to be coupled to the control component, and wherein the comparison component's signal indicates if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to a drain voltage of the power transistor.

15. (Currently amended) The current regulator of Claim 14, wherein the first switch is arranged in an open state and the second switch is arranged in an open state if the switching current flowing through the power transistor and another switching current flowing through the sense transistor ~~resistor~~ are both substantially equivalent to zero.

16. (Original) The current regulator of Claim 12, wherein the current flowing through the power transistor is substantially continuous.

17. (Currently amended) A current regulation circuit, comprising:

a means for mirroring current flowing in a sense transistor and a power transistor;

a means for sinking current that is coupled to a drain of the sense transistor, wherein the current sink pulls down a drain voltage of the sense transistor ~~resistor~~ if a current flowing through the power transistor is less than a limit;

a means for limiting the current flowing through the power transistor if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to a drain voltage of the power transistor; and

a means for presenting a signal if the drain voltage of the sense transistor ~~resistor~~ is substantially equivalent to the drain voltage of the power transistor.

18. (New) The circuit of Claim 1, wherein the power transistor is an input-side transistor of the current mirror, and wherein the sense transistor is an output-side transistor of the current mirror.

19. (New) The circuit of Claim 1, wherein the sense transistor has at least a drain, the current mirror has at least an input and an output, and wherein the output of the current mirror is the drain of the sense transistor.

20. (New) The circuit of Claim 1, wherein the current sink is arranged such that, if the current flowing through the power transistor is less than a limit the current sink pulls down the drain voltage of the sense transistor such that the drain voltage of the sense transistor is less than the drain voltage of the power transistor.

21. (New) The circuit of Claim 1, where the control circuit is further arranged to control the power transistor such that voltage regulation is performed based on the control of the power transistor.

22. (New) The circuit of Claim 1, wherein the control circuit is arranged to virtually eliminate the channel modulation effect of the current mirror without invoking a special circuit to equalize the drain-to-source voltage of the sense transistor with the drain-to-source voltage of the power transistor.

23. (New) The circuit of Claim 1, wherein the control circuit includes a comparator that is arranged to trip if a drain-to-source voltage of the sense transistor reaches a drain-to-source voltage of the power transistor, wherein the control circuit is further arranged to turn off the power and sense transistors if the comparator is tripped.

24. (New) The circuit of Claim 23, wherein the current mirror is ratioed such that the ratio of the power transistor to the sense transistor is m:1, wherein m is greater than one, the current sink is arranged to provide a current that is substantially equal to a limit current divided by m, and wherein the comparator is arranged to trip if a current at the drain of the power transistor reaches the limit current.

25. (New) The circuit of Claim 23, wherein

the control circuit is further arranged to control the power transistor such that voltage regulation is performed to provide a regulated output voltage based on the control of the power transistor, and wherein the control circuit further includes:

feedback circuitry that is arranged to provide a feedback signal based on the regulated output voltage;

feedback control circuitry that is arranged to provide feedback control responsive to a reference voltage and the feedback signal; and

a driver that is arranged to drive the gate of the power transistor.

26. (New) A regulator circuit, comprising:

a current mirror including an input-side transistor and an output-side transistor;

a current source that is coupled to a drain of the output-side transistor, wherein the current source pulls up a drain voltage of the output-side transistor if a current flowing through the input-side transistor is less than a limit; and

a control component that is arranged to limit the current flowing through the input-side transistor if a drain-to-source voltage of the output-side transistor is substantially equivalent to a drain-to-source voltage of the input-side transistor.